Robust Methodology for State of the Art Embedded SRAM Bitcell Design

M. Craig*[a], J. Petersen[b], J. Lund[a], D. Gerold[b], Nien-Po Chen[a]
[a]TestChip Technologies, Division of HPL Technologies, Inc., [b]Petersen Advanced Lithography, Inc.

ABSTRACT

A design and verification methodology of advanced SRAM bitcell design is described. Dense bitcells, drawn for embedded SRAM memory applications, are drawn and simulated for cell functionality and stability. After first-pass design, lithographic correction is determined using analytical and iterative simulation routines. Analytical corrections are tailored to comprehend not only specific tool and material platforms associated with the process technology, but are also optimized to account for process integration issues arising from mask layer to mask layer interactions. Lithography process windows are modeled though simulations based on specific stepper illumination scheme, and material systems (resist, ARC's, etc). Process integration windows are modeled through overlay of simulated patterns (e.g. contact & diffusion) while taking into account process control limits of misalignment and critical dimension (CD). Comparison of simulated to electrical bitcell results are discussed and manufacturability considerations are addressed through electrical responses of bitcell-specific diagnostic test structures.

Keywords: SRAM, bitcell, optical proximity correction, OPC, PROLITH™, lithography simulation

1. INTRODUCTION

Scaled SRAM bitcell area is a key competitive advantage for product applications requiring significant densities of embedded SRAM. To achieve industry-competitive bitcell areas, features must be drawn to design rules that are scaled beyond those of standard logic-process design rules. Effectively, numerous logic design rules are violated within the cell array. This not only requires a robust bitcell layout and simulation methodology accounting for process integration and electrical performance tradeoffs, but also demands a comprehensive lithographic correction strategy.

Since embedded bitcell design is increasingly reliant on lithographic simulation tools, it is imperative to first evaluate manufacturing margins using analytical handcrafted correction. In many cases, rules or model-based OPC/PSM generation techniques have not yet matured to produce equivalence between drawn and printed features for advanced process technologies. This is particularly true in embedded SRAM regions where different poly pitches and changes in feature periodicity, such as at interface or strapping regions, are always present. Critical pattern margins are a strong function of stepper/scanner platform and illumination schemes, ARC/photoresist selection, and mask processing. As a result, automated correction routines on initial bitcell / product designs provide inadequate process margins and insufficient manufacturing yield of embedded SRAM IP.

Higher quality embedded SRAM IP and faster times to yield entitlement are key milestones that can be achieved by using a phased bitcell development approach. In this work, we demonstrate a bitcell development schedule for rapid cell design and manufacturability. This approach consists of first pass cell design, electrical simulation for stability analysis, lithographic simulation, and electrical evaluation of optimized bitcell designs.

2. MOTIVATION & CELL DESIGN

Bitcell areas are targeted based on product application. Key technical tradeoffs including area, power, cell current, static noise margin, and manufacturing margins must all be considered when optimizing cell designs. Ultimately, bitcell device sizes and intra-cell feature dimensions are derived from a proper balance of each of these key technical care-

abouts. As such, a comprehensive lithographic strategy is imperative to not only enable time-zero bitcell functionality, but to also provide manufacturable process margins in the larger process flow.

Fundamental cell functionality considerations must be addressed in conjunction with lithographic correction strategies. In particular, static noise margin (SNM) must be considered as a key figure-of-merit of bitcell robustness. Figures 1 and 2 illustrate a standard six-transistor (6-T) bitcell schematic [1] and corresponding simulated "butterfly" curves. Separation of these curves (SNM) indicates noise immunity of the bitcell to disturb events during circuit read operations. Figure 3 illustrates simulated and electrically measured curves as obtained from an un-optimized bitcell in the present work. An asymmetrical response can be seen in the electrical results, indicating a mismatch in inverter behavior between each side of the bitcell. These inherent asymmetries, resulting from device mismatch events, reduce the overall noise immunity of the bitcell to that of the lowest SNM value of the measured response. Cell current (Icell), also a key figure-of-merit for circuit read performance, may be negatively affected by such mismatch issues. To address these degradation events, several design and process interactions must be evaluated in the context of lithographic correction. Uncorrected diffusion, poly, and contact features, shown in figure 4, illustrate front-end layout geometries of the cell electrically described in Figure 3. It can be observed that several process interactions may give rise to electrical mismatch described earlier. SNM degradation results from PFET or NFET mismatch across left and right sides of the bitcell, and may be induced from several process integration effects. Specifically, rounding of PMOS and NMOS diffusion features at inner feature "elbow" regions combined with poly misalignment to diffusion can lead to device mismatch and SNM reduction. In addition, simple CD mismatch due to feature-dependent printing variation can result in similar device asymmetries. Figure 5 illustrates simulated SNM responses as a function of pull-down device mismatch. Plotted mismatch percentages are relevant values based on CD and overlay tolerances generally allowed by the manufacturing process. In this case, a 15% device mismatch event roughly corresponds to a 20nm and 30nm CD excursion from target, in poly and diffusion levels, respectively. It is observed that SNM degradation of 10% is observed for this level of device mismatch. Since SNM is a key metric for robust bitcell design, a comprehensive lithographic correction scheme must be employed to specifically address process and design interactions that may lead to marginal bitcell performance.

In addition to cell stability, one must consider manufacturability of scaled bitcells. In this work, critical pattern levels including diffusion, poly, contact, and metal-1 have been optimized to exhibit robust manufacturing margins. Figure 6 illustrates uncorrected layout in an array context of diffusion, poly, and contact layers. Specific regions are highlighted which must have feature corrections optimized against different technical constraints. In the case of the poly mask level, poly enclosure of diffusion must be maintained while being isolated from the near-neighbor wordline poly feature. Similarly, interior diffusion "elbows" must be corrected to mitigate gate-widening effects in cases of poly misalignment to diffusion. For the contact level, diffusion features must be optimally corrected to provide robust contact area while not reducing process margins associated with diffusion-to-diffusion isolation capability. These multiple constraints must be concurrently satisfied and must provide margins adequate to accommodate allowable manufacturing spec limits. Manufacturability considerations in addition to time-zero bitcell functionality concerns must be addressed by the same overall lithographic correction strategy.

In this work we have targeted embedded bitcell designs to areas less than or equal to 70% of the area allowed by minimum logic design rules. Further, we have targeted each cell to manufacturable electrical design targets including SNM's of at least 280mV Icell of 60 to 70uA. Having defined first-pass cell layouts to achieve these goals, the process of analytical lithographic correction is started.

3. SIMULATION APPROACH

The process for correcting a bit cell is shown in Figure 7 and is described as follows. First, it is important to define the boundary conditions for the device and for the fabrication process. As will be shown later, the six poly transistors and the gaps between poly pads had no common critical dimension (CD) size focus-exposure process window corridor; so extensive correction is required. In addition, for optimal performance, uniform gate width across active areas needs to be maintained. Further, the gate line end cannot fall into active and the poly cannot encroach active or other poly areas. Next, the active pattern must maintain a uniform width under the poly gates. Contacts must stay open but not so large

that they fall off the pads of active, poly, and metal. Metal-1 should cover the contacts completely with out encroaching other metal features. For the process, an audit is conducted to learn imaging capability, process biases and to gather information needed to calibrate the lithography simulators with the highest precision and accuracy possible. This means gathering linewidth data for various pitches and process conditions and, in an ideal situation, using the CD data and measured values for dose and focus to calibrate physical chemical data about the resist and to extract characteristic aberrations for the imaging system. Since the ideal rarely happens, linewidth data and information from the resist supplier to build a model is often used and we assume an aberration-free, diffraction-limited exposure system. Doing this is often inadequate so if it is at all possible, CD data from the fab must be used for best possibility of success. Regardless, once the imaging conditions are known and the calibration of the lithography models are complete, the work of optical proximity correction can be done.

In this work, we used the unpolarized vector model and resist models of PROLITH™ 3D v7.1.1. To reduce cycle time we distributed PROLITH across thirteen computers whose simulation instructions are spawned and results collected by a single master computer using ProLE™ (tariat) interface that we (PAL, Inc.) have co-developed with Jeff Byers of KLA-Tencor, Austin, TX. Using the AutoTune module of KLA-Tencor's ProDATA™ v1.3, photoresist parameters were extracted by fitting resist vendor focus-exposure CD data with PROLITH models. Simulation conditions were set using inputs from the wafer manufacturer including illumination scheme, resists used at diffusion, poly, contact and metal-1 levels, ARCs, film thicknesses, reflectivities, etc.

Then, with the calibrated models, optical proximity correction began. Corrections were made in an iterative fashion using two types of simulations. The first is a large grid overview of 2 X 1 bit cell for roughing in the required OPC per layer. The large grid size was typically 5% to 10% of the smallest CD. For refinement, we used multiple metrology sample cuts and small grid simulation regions of grid-steps equivalent to less than 1% of the critical feature to simulate CD response to variations in focus-exposure conditions. We then searched for common process corridors using ProDATA. At poly, we monitor three sample cuts for each transistor positioned at the edges and middle of each underlying active area and the space between the poly pad and the next transistor pad for a total of eighteen sample cuts. This is shown in Figure 8. Likewise, at active, we monitor two to three sample cuts in the gate region. For contacts, we monitor the size of each contact. For metal, we visually monitor the areas that overlay the contacts. Once we generate a set of reasonable corrections per layer, we then use ProDATA to do a layer-to-layer overlay analysis of various focus-exposure conditions and then visually interpret critical shape interactions between the layers, making measurements by hand where necessary.

In this work, at every step of the process, we used biasing width and height of features, serifs and hammerheads to make sizing corrections. To print a proper regular rectangular shape at the wafer, the transistors have a trapezoidal shape on the mask. This structure is made using successively larger rectangles that result in many sub-resolution jogs on the mask pattern. Interviews with several mask makers revealed that these jogs should be kept less than 10nm to avoid triggering false defects during the mask inspection and repair processes.

4. SIMULATION RESULTS

The focus-exposure process widows for all sample regions for the un-corrected poly are shown in Figure 9. As mentioned earlier, there is no common process window that holds the respective CD measurements to a ±10% target. Figure 10 looks at this differently by using a bar graph of dose to size for each of the sampled features. To provide correction we first partition the transistors into several rectangles and run a sizing matrix of all rectangles to find a combination that gives uniform sizing for a range of focus and exposure conditions; then we use a similar process for the pad regions, then combine and rebalance as necessary. Figure 11 shows the process window after one iteration and figure 12 shows them after the final iteration. A manufacturable process corridor for all features is created following this final iteration. Figure 13 illustrates the simulated features at uncorrected, intermediate correction, and final correction stages.

This process is then repeated for diffusion, but in this case, along with biasing we use serifs and anti-serifs to produce the desired image shape. Figure 14(a) shows an overlay of the mask pattern without and with correction; and figure 14(b) shows an overlay of the resist images with and without correction. Figure 15 shows the corrected poly overlaid with

diffusion at the optimal focus and exposure. Note how the curvature of the active causes the overlapped regions to lose their rectangular shape. However, as shown in Figure 16, with the corrected diffusion layer, the proper shape is maintained throughout the device space.

Other than defocus, we have not considered aberrations in this analysis. This is not preferred, however, in the absence of lens data, we can develop hypothetical aberrations for further refinement of the design. This should be done if the diffraction pattern of each critical feature samples different parts of the lens because of pitch variations or because of illumination changes between layers or if the same portion of the lens is sampled but the weighted average of the aberration changes because of change in duty cycle within the device pitch.

Next, contacts are shown. Figure 17 shows simulated bitcell contacts. Figure 18 shows the common process window for biased-up contacts and Figure 19 shows for non-biased contacts. Under these conditions, the non-biased contacts yield the best result. This is true if side-lobes do not print. PROLITH examination in figure 20 shows that this is the case by overexposing the resist 75% from nominal (at best focus), and examining the contacts for side-lobe printing by looking at the top the resist and then by taking different z-slice samples from where side-lobes are present until they are no longer evident. Since the non-biased contacts met their process window requirements, no further optimization was made. Optimal condition overlay with active and poly are shown in figures 21 and 22, respectively.

For metal-1, bias, notch and serif corrections were made by hand. Our success criteria was non-critical, the metal should provide total contact coverage and should not bridge with other metal features.

5. ELECTRICAL RESULTS & DISCUSSION

First order yield and e-test results are shared as a first metric of the analytical correction approach. Table I includes yield comparison of several dense, corrected bitcell designs to that of a nominal design rule-compliant, uncorrected bitcell. In this work, dense bitcell designs are targeted for embedded SRAM applications, and are designed to an area less than or equal to 70% that of the uncorrected, nominal rules bitcell. It is seen that yield of cell Y, drawn at 30% smaller area dimension is equivalent to that of the logic-rules compliant bitcell. However, cell Z, scaled to a 40% area reduction exhibits a markedly reduced yield response. From parametric test findings, it is confirmed that this yield loss is not due to inadequate correction in critical pattern layers. Rather, it results from several unrelated process integration issues that encounter limits of the process capability for this scaled cell area.

To monitor critical features corrected within each embedded bitcell design, a number of bitcell topology-like test structures were designed to isolate possible failure points. These structures are designed to electrically characterize the fundamental design trade-offs within the corrected bitcell footprint. A key example is the ability to effectively create a pull-down FET gating event by adequate poly enclosure of diffusion, while simultaneously isolating latch gate poly from the near-neighbor wordline. Additional examples include isolation of contact features from poly gates, metal-1 isolation to near-neighbor features, and contact integrity at minimally enclosed diffusion and poly contact regions. For consideration of each failure mode, a test structure response is monitored for process capability evaluation. Figures 23 and 24 illustrate a test structure design testing bitcell poly-to-poly isolation and its electrical test response, respectively. Tightly distributed and low current levels indicate robust isolation capability resulting from an adequate feature correction. Similarly, figures 25 and 26 demonstrate electrical test responses as indicated by structures designed to characterize poly to contact isolation margin and metal-1-to-metal-1 isolation capability. Results in each case indicate the bitcell design affords parametric yield margins consistent with full circuit die yield comparable to the larger, design rule compliant bitcell.

Finally, discrete bitcell testers were characterized to investigate electrical design margins of the various cell designs. Figure 27 illustrates overlaid butterfly curves from each of the dense cell designs, Y and Z. Slight asymmetries in the response reduce the SNM of each cell to the lowest value of noise margin on either left or right sides of the butterfly response. Based on electrical test results, this asymmetry is largely due to misalignment effects in the manufacturing process rather than linewidth control of the patterning processes.

6. CONCLUSION

Use of a comprehensive analytical correction methodology has shown to be effective for achieving scaled-area SRAM bitcell designs. Because this methodology takes into account the entire pattern transfer system including tooling and materials, it can be used to demonstrate manufacturable embedded cell designs, and may also be used for verification of rules or models-based automated OPC routines.

7. REFERENCES

1. A. Bhavnagarwala, et al, IEEE J. of Solid State Circuits, Vol. 36, 4, pp. 658 -665.

* mcraig@testchip.com; phone 1 512 997 1301; fax 1 512 997 1399; http://www.testchip.com

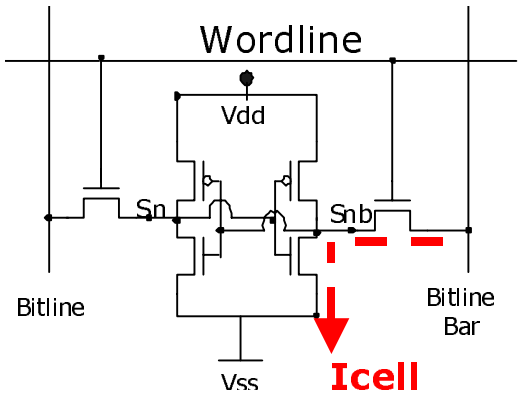

Figure 1: Standard 6-T SRAM bitcell schematic

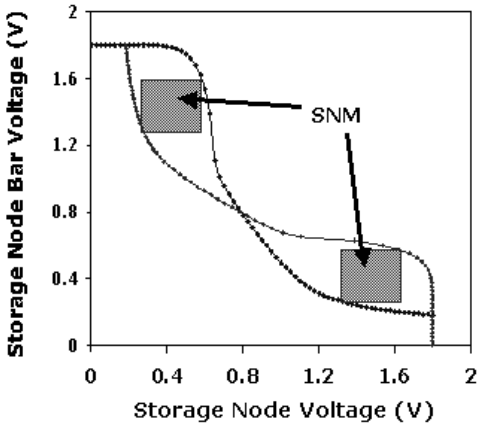

Figure 2: Butterfly curve indicating static noise margin (SNM) of SRAM bitcell.

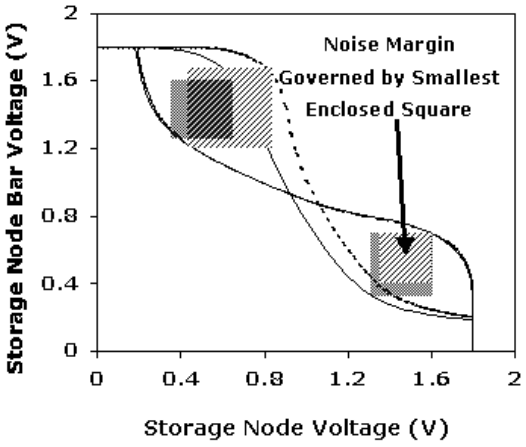

Figure 3: Asymmetry in bitcell SNM response resulting from inherent process variation.

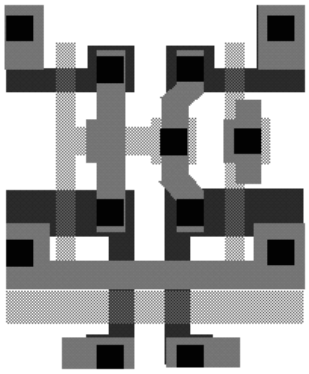

Figure 4: SRAM bitcell layout. Circles indicate critical points for OPC to retain cell margin.

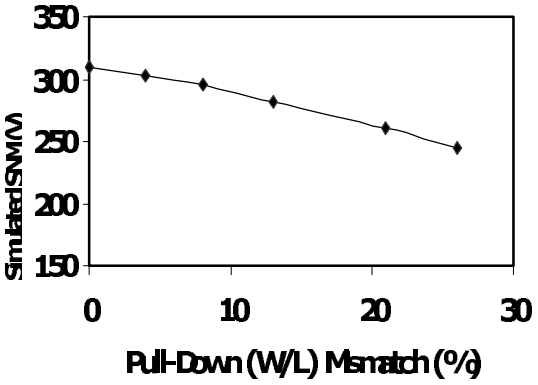

Figure 5: SNM degradation resulting from pull-down device mismatch induced by CD offset or overlay

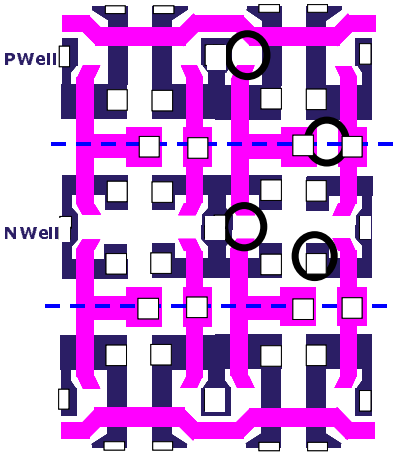

Figure 6: Uncorrected cell array. Black circles indicate several critical correction points.

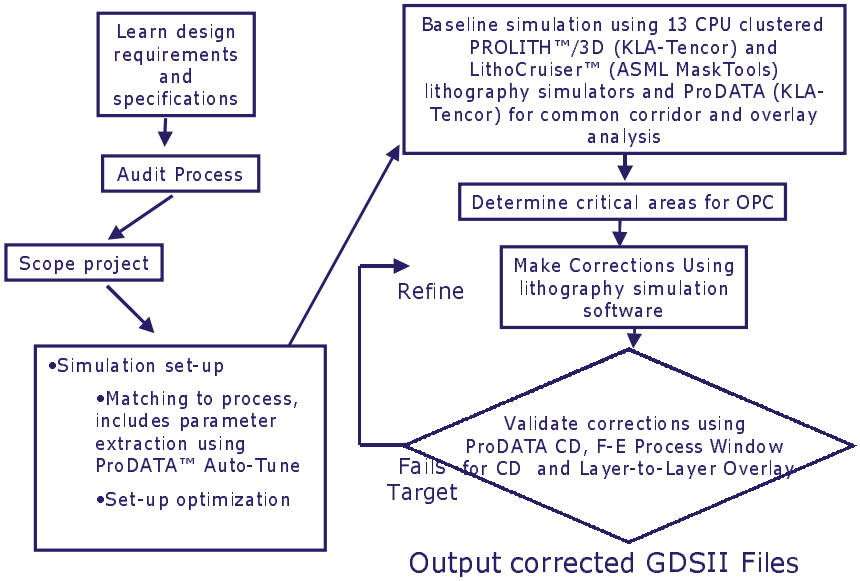

Figure 7: Simulation methodology for analytical correction

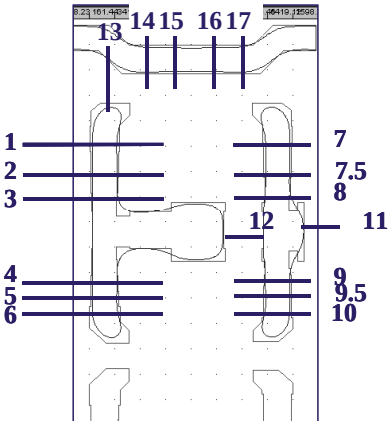

Figure 8: Sample cuts for each transistor positioned at edges & middle of device. Inter-feature spacings also show window for all uncorrected poly sample cuts.

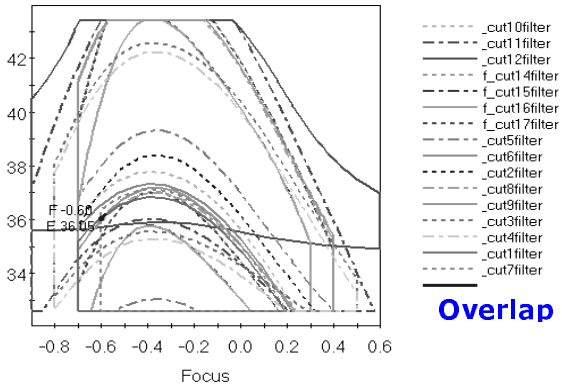

Figure 9: No focus/Exposure process

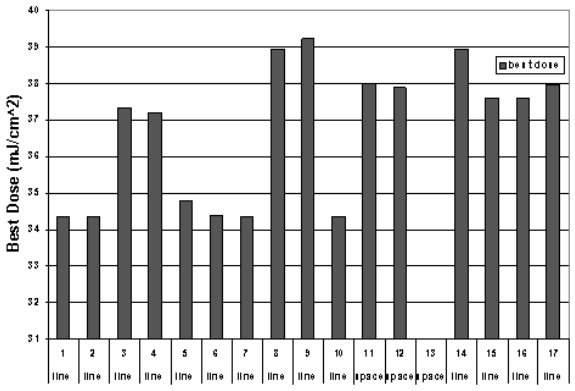

Figure 10: Optimal dose required at each cut to achieve desired feature CD.

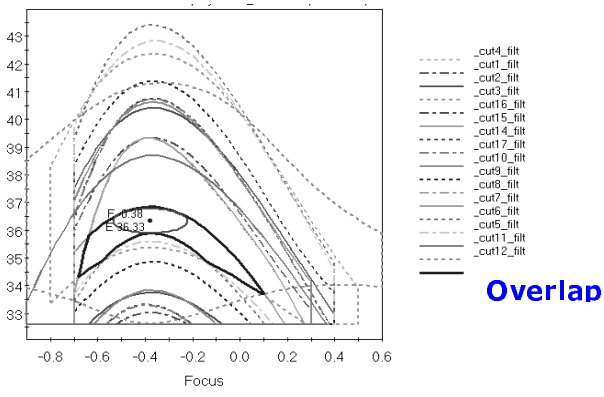

Figure 11 Focus/exposure window after first poly correction iteration.

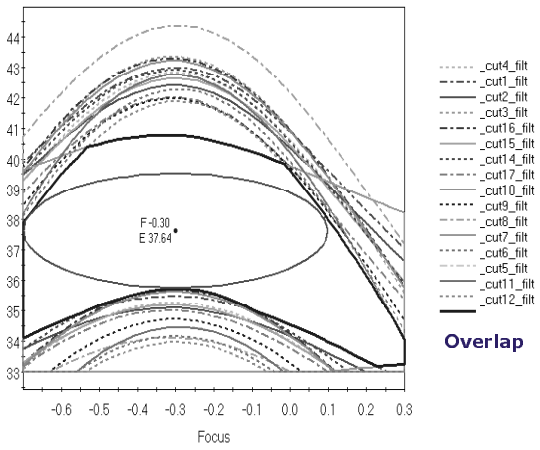

Figure 12: Focus/exposure window after final correction iteration.

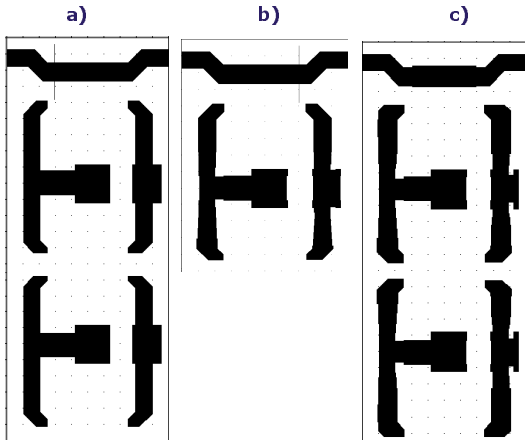

Figure 13: Poly features a) uncorrected, b) first correction, c) final correction.

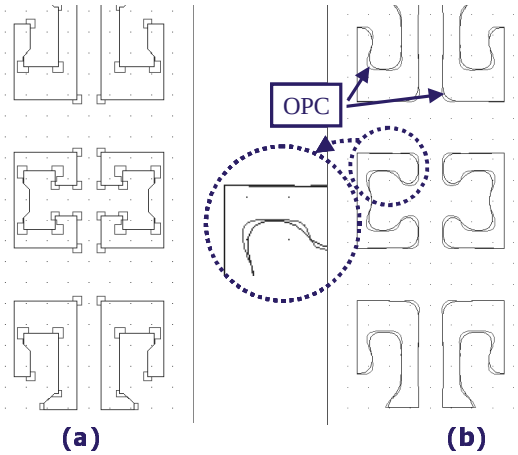

Figure 14: (a) Diffusion mask pattern with & without correction; (b) Simulated resist pattern of same

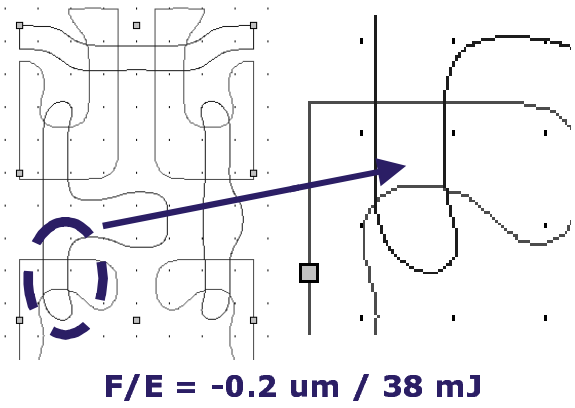

Figure 15: Corrected poly overlay with uncorrected diffusion at optimal F/E condition.

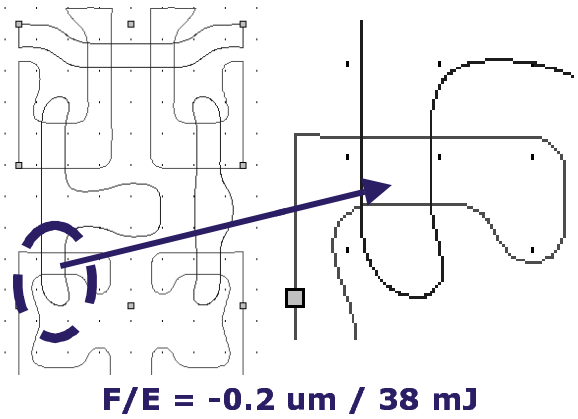

Figure 16: Corrected poly overlay with corrected diffusion at same F/E condition from figure 15.

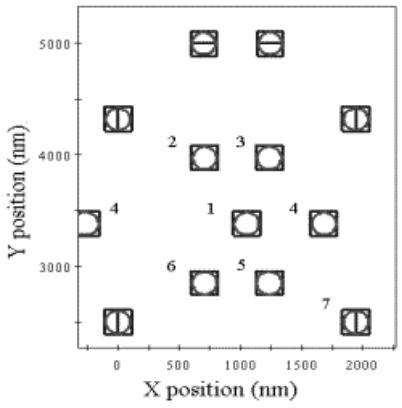

Figure 17: Drawn and simulated resist images of bitcell contacts

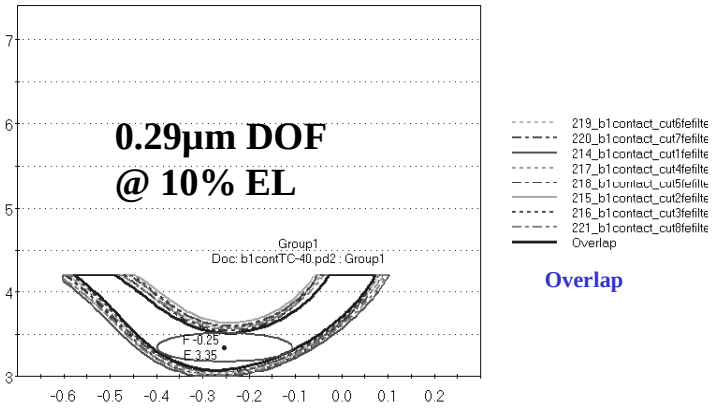

Figure 18: Common process window for 40nm upsized contacts.

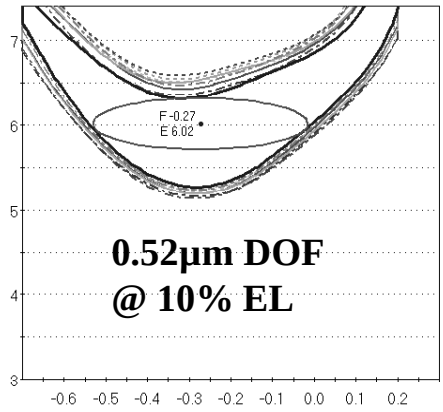

Figure 19: Common process window for un-biased contacts.

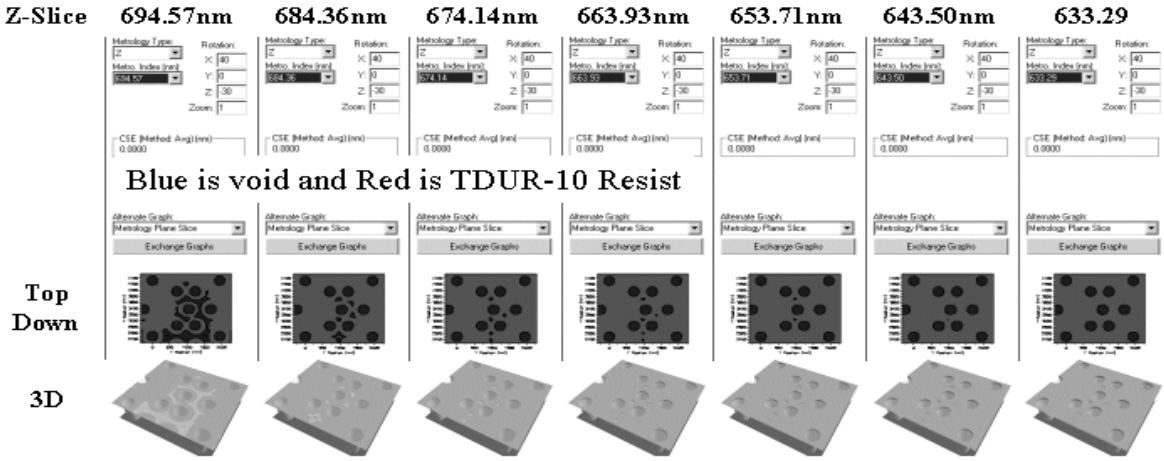

Figure 20: Resist film thickness z-slices of contacts that were 75% overexposed from nominal.

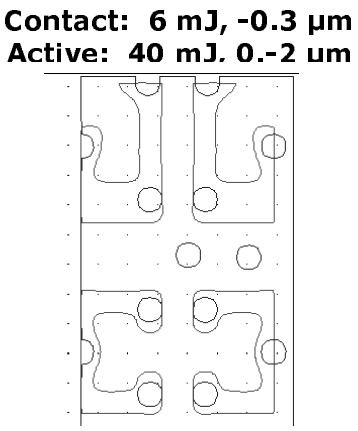

Figure 21: Optimal diffusion and contact Resist image overlay

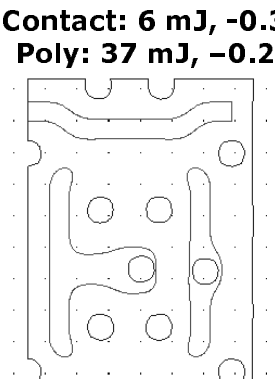

Figure 22: Optimal poly and contact resist image overlay

Bitcell	X (Nom)	Y	Z
Yield (% of Nominal)	1	1	0.26
Area (% of Nominal)	1	0.7	0.6

Table 1: Normalized yield versus cell area

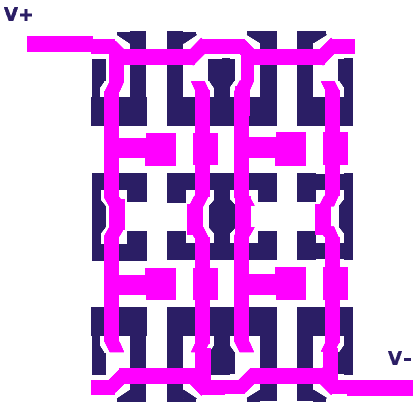

Figure 23: Poly to poly isolation tester

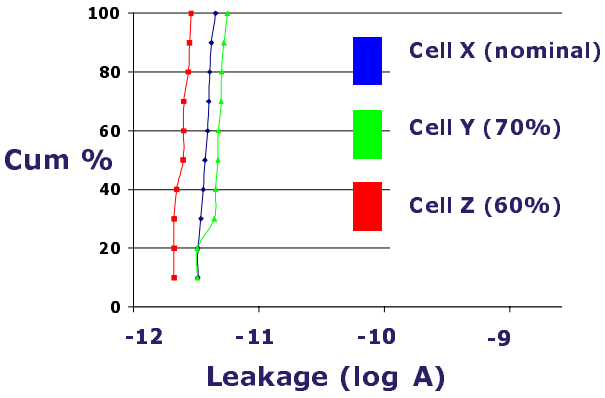

Figure 24: Poly to poly isolation versus cell type.

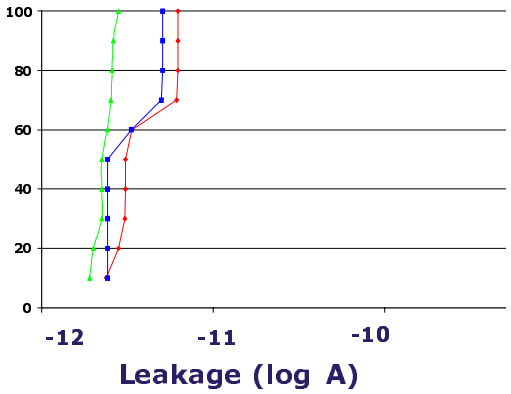

Figure 25: Poly to contact isolation versus cell type

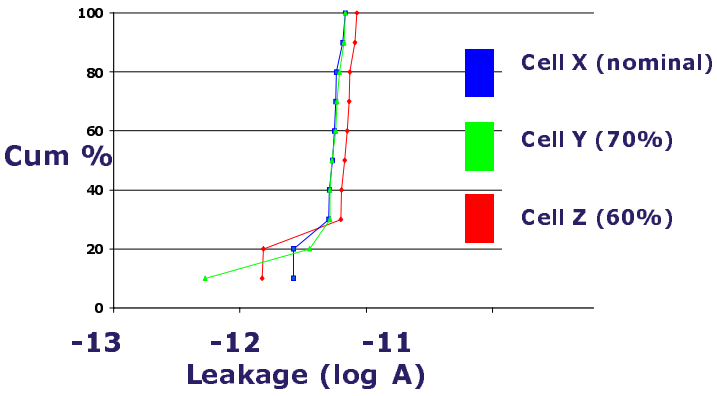

Figure 26: Metal-1 to metal-1 isolation versus bitcell type

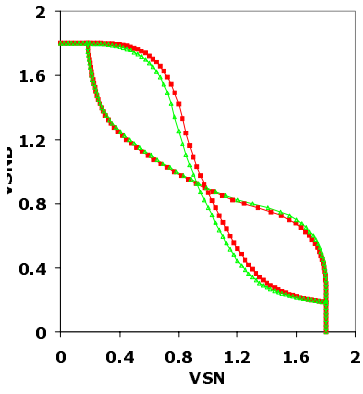

Figure 27: Butterfly curves of scaled area bitcells indicated slight asymmetry derived from misalignment.