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Considerations for the Use of Application-Specific Photoresists

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ABSTRACT

In recent years, photoresist suppliers have migrated to offering a full palette of resist chemistries and processes which are specifically tailored for particular pattern types and / or exposure processes. Thus we now see designations such as “contact resist”, “isolated line resist”, “dense line resist”, “attenuated phase shift resist”, etc. This specialization offers the lithographer more choices for continual performance improvement and optimization, but implementation of multiple resist platforms in manufacturing can be problematic. In this paper, we examine the design criteria and efficacy of pattern- and application-specific photoresists versus a generic “multi-purpose” material, and identify some of the trade-offs which can be expected when employing these resists. Generalized ideal resist behaviors are presented for different pattern criteria, including proximity bias. Both experimental and simulation results are given.

Keywords: Keyword: photoresist, isolated line, dense line, contact hole, DUV, I-Line, contrast, develop

1. INTRODUCTION

The rapid evolution of semiconductor technology over the past 15 years has been fueled in large part by advances in photolithography. Improved lens design and manufacturing capability has leveraged the fundamental physics governing the formation of the aerial image, which carries the mask information to the wafer. Thus we have realized concurrent wavelength reduction and numerical aperture increases with overall improved image control across the full field at ever-decreasing critical dimensions (CD). These decreasing dimensions have been further enabled by the physics of phase shift masks and off-axis illumination. The role of chemistry, however, has been equally vital, as improved photoresist chemical systems have allowed manufacturing at k_1 factors previously thought impossible. For instance, I-line resists, once thought incapable of running 350 nm processes are now routinely doing 300 nm processes and in some cases being proposed for 250 nm processes. An interesting trend resulting from these chemistry improvements has been the migration from “one size fits all” resist chemistries to pattern-specific formulations. This has been enabled by a number of innovations and improvements including polymer synthesis and molecular weight fraction isolation, new photoactive compound (PAC) and photoacid generator (PAG) types, as well as an improved overall understanding of the structure-property relationships which dictate the final dissolution rate versus exposure function. For chemically-amplified DUV resists, the composition trend has been away from simple [polymer, PAG, solvent] to specific molecular weight resin distributions featuring multiple acid-labile protecting groups, mixtures of different transparency PAGs, and a variety of base additives dissolved in solvent mixtures.

Today’s leading-edge six level metal 180 nm CMOS logic processes feature 25-30 masking layers patterned by a mix-and-match combination of I-line and DUV exposure tools. Table 1 shows representative pattern layers and the associated photoresist requirements fulfilled by the 2 I-Line and 1 DUV resists. Within five years, leading edge factories will likely feature I-line, DUV, and 193 nm wavelengths, thus adding to the complexity of the overall photoresist arsenal. As each new lower wavelength technology proliferates, photoresist suppliers have introduced appropriate chemistries with the requisite optical absorption and sensitivity properties. The result has been a significant growth in the number of different chemistries which they must offer. Figure 1 shows the growth in number of photoresists offered at any given time by a representative supplier for each of the exposure wavelengths. The total number of resists appears to follow a type of Moore’s Law, nearly doubling every five years. Resist supplier roadmaps have become an exceptionally complex menu of niche products, with both wavelength and pattern-specific offerings.

As shown in Table 1, in the case of DUV lithography today, critical mask levels typically include active, gate, local interconnect, contact, and first metal. The exact CD and minimum pitch of these layers are of course product-specific, but in general, a distinction has often been made between memory and random logic designs. Cost-competitive memory designs require the smallest possible bitcell layout and thus force patterning of minimum pitch features, while random logic designs do not feature the periodicity which allows small pitch. It is important to note, however, that memory designs often include critical periphery circuitry which is largely isolated, and the trend in system-on-a chip integration is to include both memory and logic functionality in the same design. Thus the bifurcation of "isolated" and "dense" line resist types is somewhat inappropriate. Nevertheless, this differentiation is often highlighted by photoresist suppliers, and deserves exploration. We explore here the optimum generalized characteristics for imaging such feature types.

2. EXPERIMENTAL

Simulations were conducted using PROLITH v 6.04 from FINLE Technologies. A theoretical DUV photoresist was used. Table N gives the baseline parameters for the photoresist. A fixed NA of 0.50 with $\sigma = 0.60$ was used for all simulations.

Experimental top SEM data was analyzed using PRODATA from FINLE Technologies to obtain exposure latitude versus DOF plots. K2G, M54Y, 1095, UV5, TMX1062…

Consider binary, alt PSM, conv OAI for N= 2-100

Also need to run contacts 0.250 contacts, 0.22 contacts dense and iso

Can also look at different Rmin, Rmax for a given N

Experimental results, compare perhaps UV5 with M54Y for gate and LI. Get K2G, UV5, M54Y .
Can show gate, LI data

3. RESULTS

A comparison was made of the process window for 250, 180, and 150 nm features, on either 500 nm or 1000 nm pitch. For each feature type, the resist develop contrast, N, was varied from 2 to 20. The resulting exposure latitude versus DOF plots are shown in Figure N. It can be seen that in all cases, regardless of target linewidth or proximity, the exposure latitude at best focus improves with increasing develop contrast. It can also be seen that for all 500 nm pitch features, the DOF improves with increasing develop contrast. The situation is different, however, for isolated lines, where the preferred maximum DOF contrast increases from 2 at 250 nm to 3 at 180 nm to 5 at 150 nm.

The proximity bias (1000 nm pitch CD - 500 nm pitch CD) is shown in Figure N for the three feature sizes at various develop contrast values. In general, higher contrast resist results in greater bias, but depends upon the target CD. 250 nm featues, for instance show 0 bias for a develop contrast of approximately 8, while 150 nm isolated features size larger than the 500 nm pitch feature regardless of contrast.

These results can be interpreted in terms of the aerial images shown in Figure N.

While measurable process lattitude improvements may in some cases be realized by using a custom resist per layer, there are practical cost of ownership limitations to the number of different materials which can be implemented in a manufacturing environment. This is particularly true if the photoresists require different bake conditions, which can dramatically effect the availability of the track for production as bakeplates equilibrate to temperature setpoints. Additionally, the time required to daily qualify resist processes as well as new batches of multiple materials takes away from production time. Finally, in the absence of full automation, more chemicals represent increased opportunity for human error associated with managing multiple chemicals. Some amount of tool-level dedication can alleviate the challenges associated with multiple resist platforms, but in the case of DRAM production, tools are often dedicated to lots, not levels, thus increasing the difficulty.

4. SUMARY

REFERENCES

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2. Petersen, J., McCallum, M., Kachwala, N., Socha, R., Chen, J., Laidig, T., Smith, B., Gordon, R., Mack, C., BACUS Symp. 1998.
3. blah
4.

Table 1. Typical 180 nm CMOS Logic Process Photoresist Requirements

Layer	l (nm)	Resist	Thickness (nm)	Requirements
Active	248	D_1	700	Semi Iso Space resolution
S/D	365	I_1	3000	High transparency, photospeed
Gate	248	D_2	500	Semi Iso Line resolution, ARL compatable
Local Interconnect	248	D_1	700	Semi Iso Space / Contact resolution
V_t adjust	365	I_2	1000	High photospeed
Contact	248	D_1	800	Hole resolution
First Metal	248	D_1	800	Dense Line/Space resolution
First via	248	D_1	800	Hole resolution
Metal 2-N	365	I_2	1000	Dense Line/Space resolution
Via 2-N	365	I_2	1000	Att PSM surface inhibition
Final Metal	365	I_2	1500	High transparency, photospeed
Passivation	365	I_1	3000	High transparency, photospeed

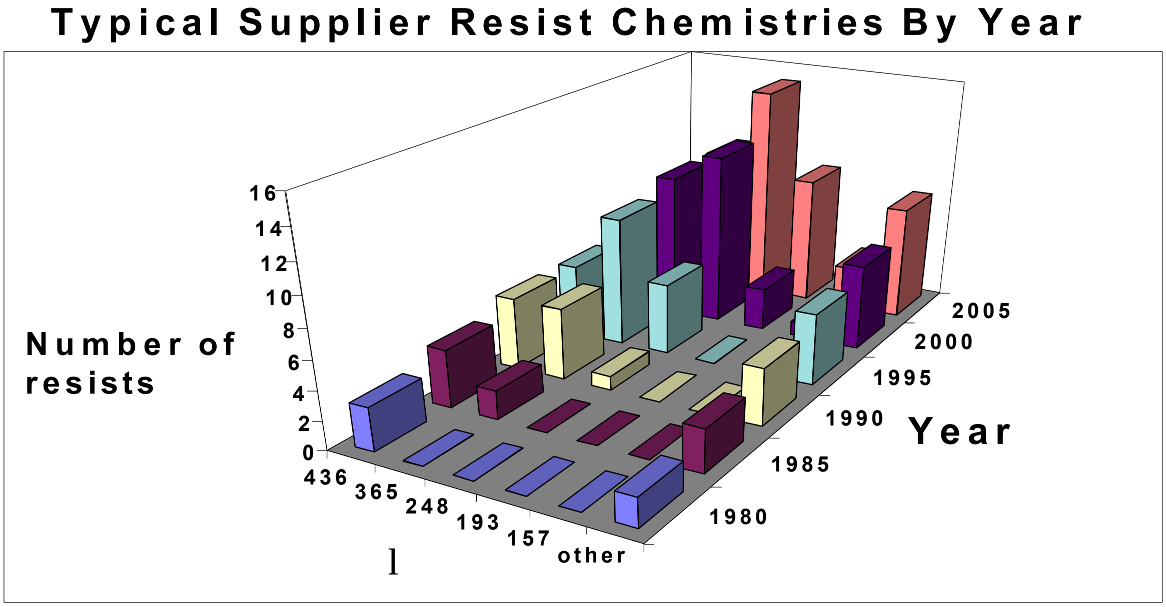
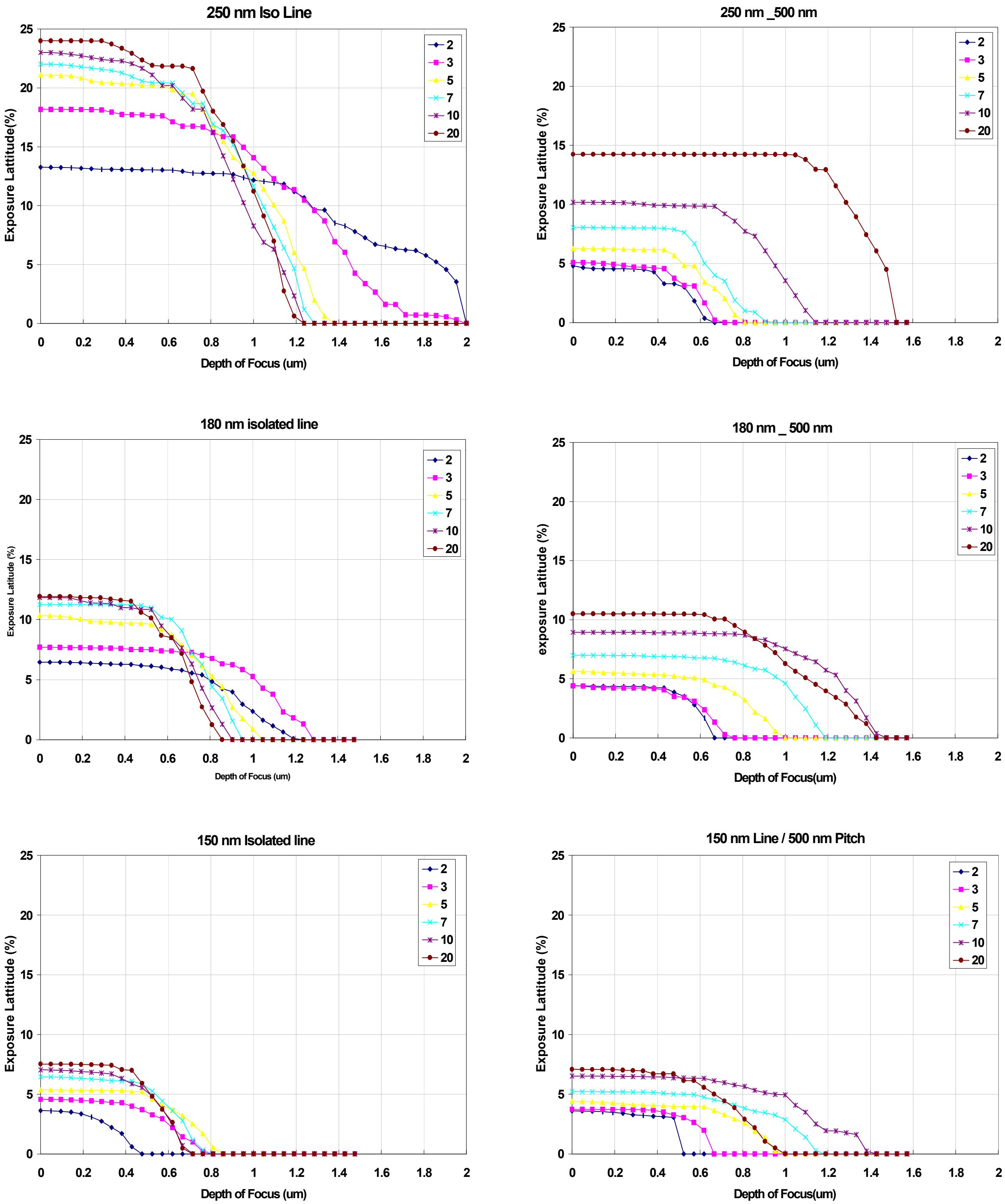


Figure 1. Growth in the number of different resists offered by a typical supplier since 1980, grouped by exposure wavelength.


250 nm Iso Line
Exposure Lattitude(%)
Depth of Focus (um)
250 nm _500 nm
Exposure Latitude (%)
Depth of Focus (um)
180 nm isolated line
Exposure Latitude (%)
Depth of Focus (um)
180 nm _ 500 nm
exposure Latitude (%)
Depth of Focus(um)
150 nm Isolated line
Exposure Lattitude (%)
Depth of Focus (um)
150 nm Line / 500 nm Pitch
Exposure Lattitude (%)
Depth of Focus(um)
2
3
5
7
10
20
0
5
10
15
20
25
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

FigureN.

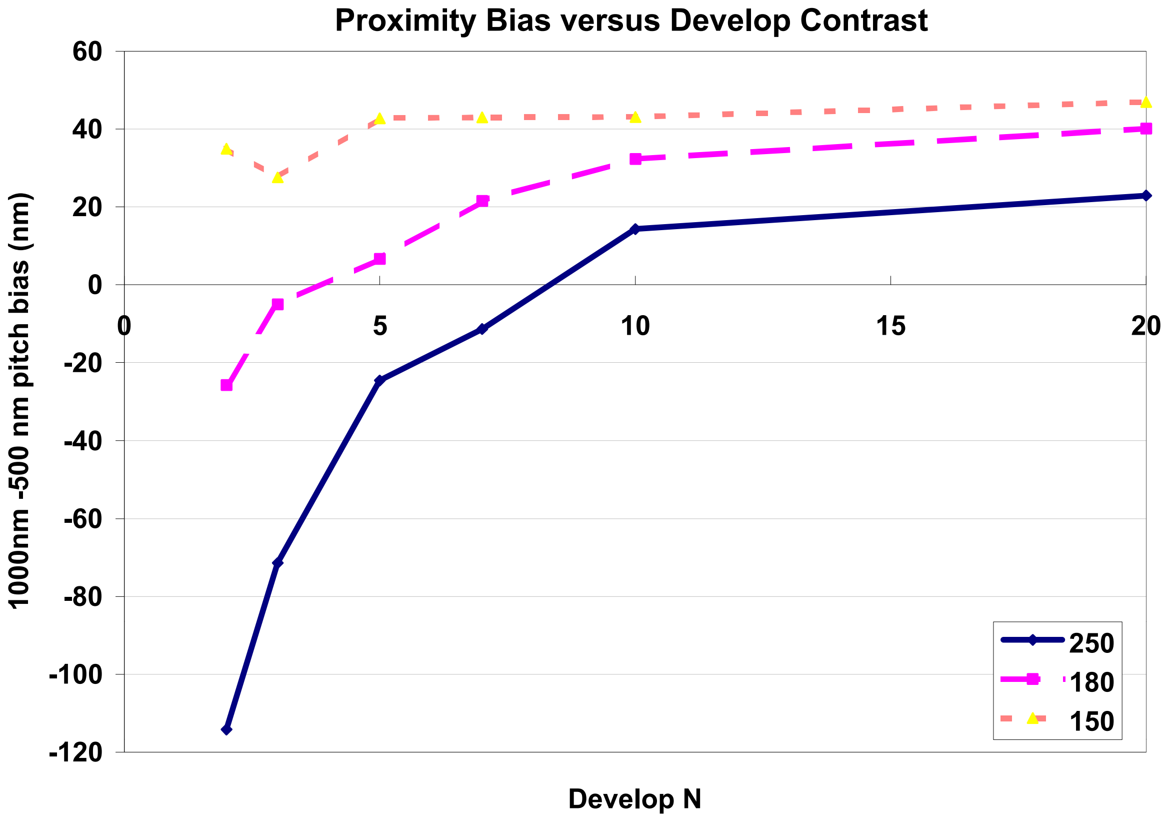
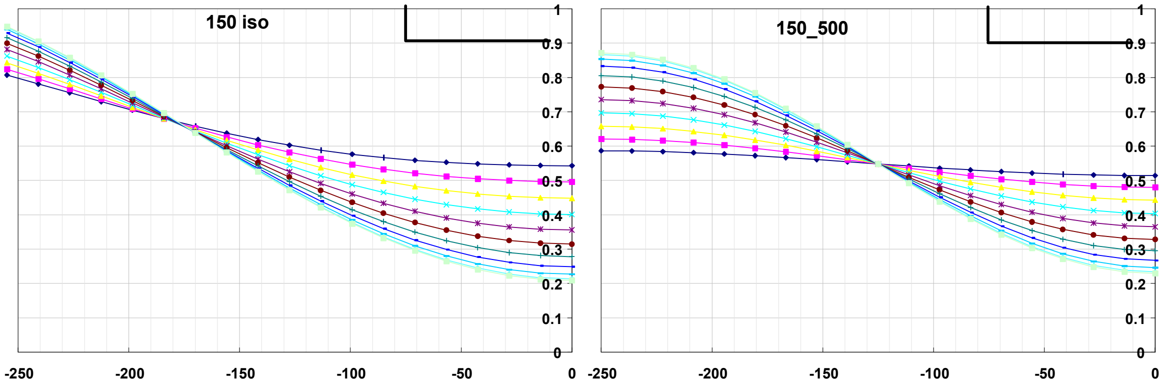

Proximity Bias versus Develop Contrast
1000nm -500 nm pitch bias (nm)
60
40
20
0
-20
-40
-60
-80
-100
-120
0
5
10
15
20
Develop N
250
180
150

Figure N.


150 iso
150_500
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-250
-200
-150
-100
-50
0

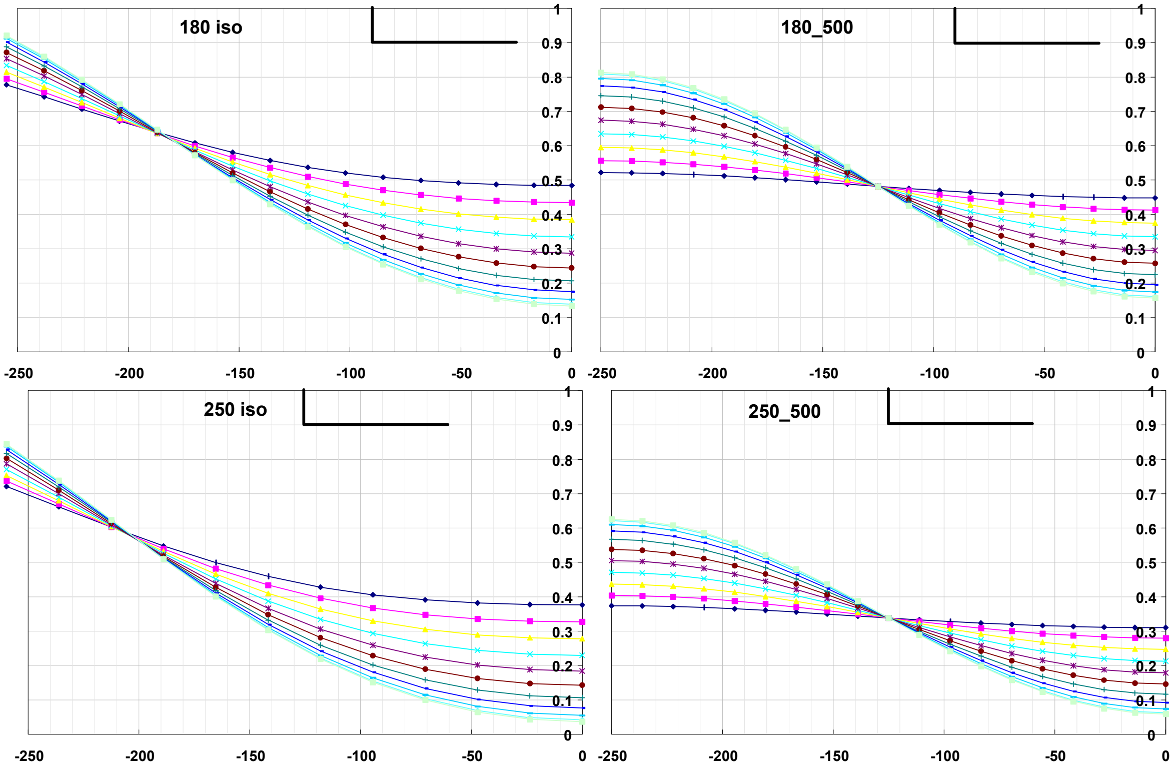
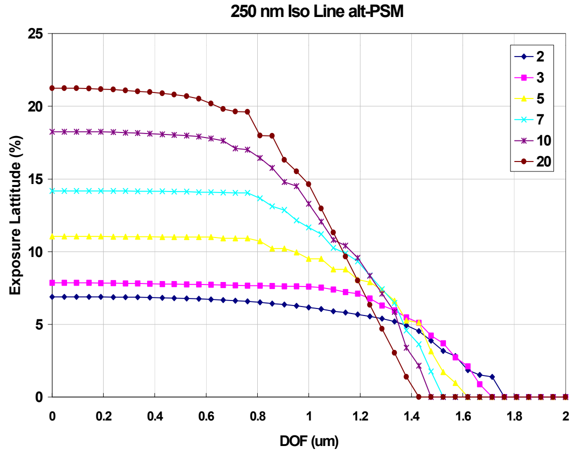
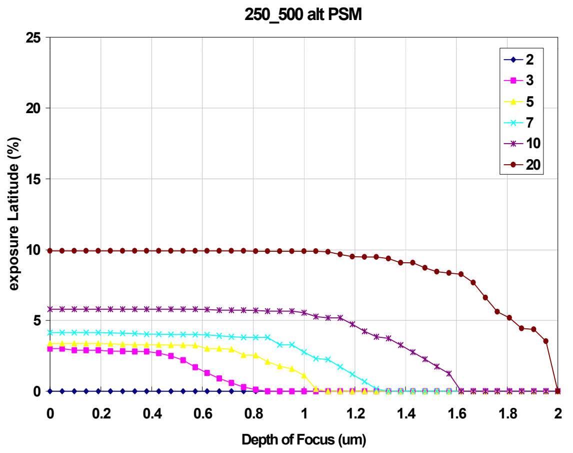
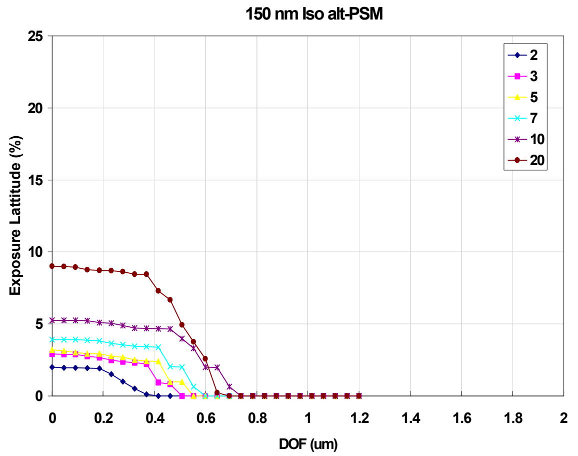
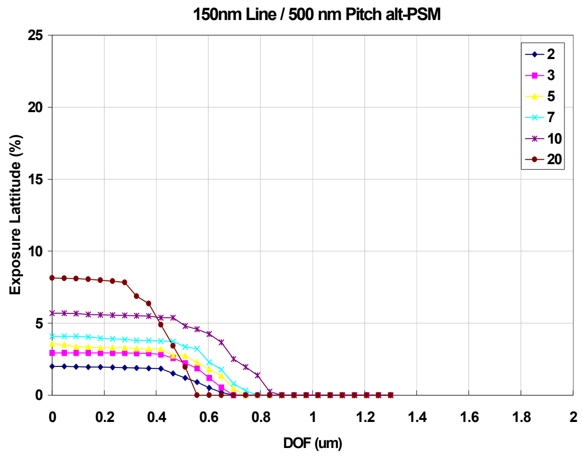

180 iso
180_500
250 iso
250_500
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-250
-200
-150
-100
-50
0

Figure N.


250 nm Iso Line alt-PSM
Exposure Lattitude (%)
DOF (um)
25
20
15
10
5
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
2
3
5
7
10
20


250_500 alt PSM
exposure Latitude (%)
25
20
15
10
5
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Depth of Focus (um)
2
3
5
7
10
20


150 nm Iso alt-PSM
Exposure Lattitude (%)
25
20
15
10
5
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
DOF (um)
2
3
5
7
10
20


150nm Line / 500 nm Pitch alt-PSM
Exposure Lattitude (%)
25
20
15
10
5
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
DOF (um)
2
3
5
7
10
20